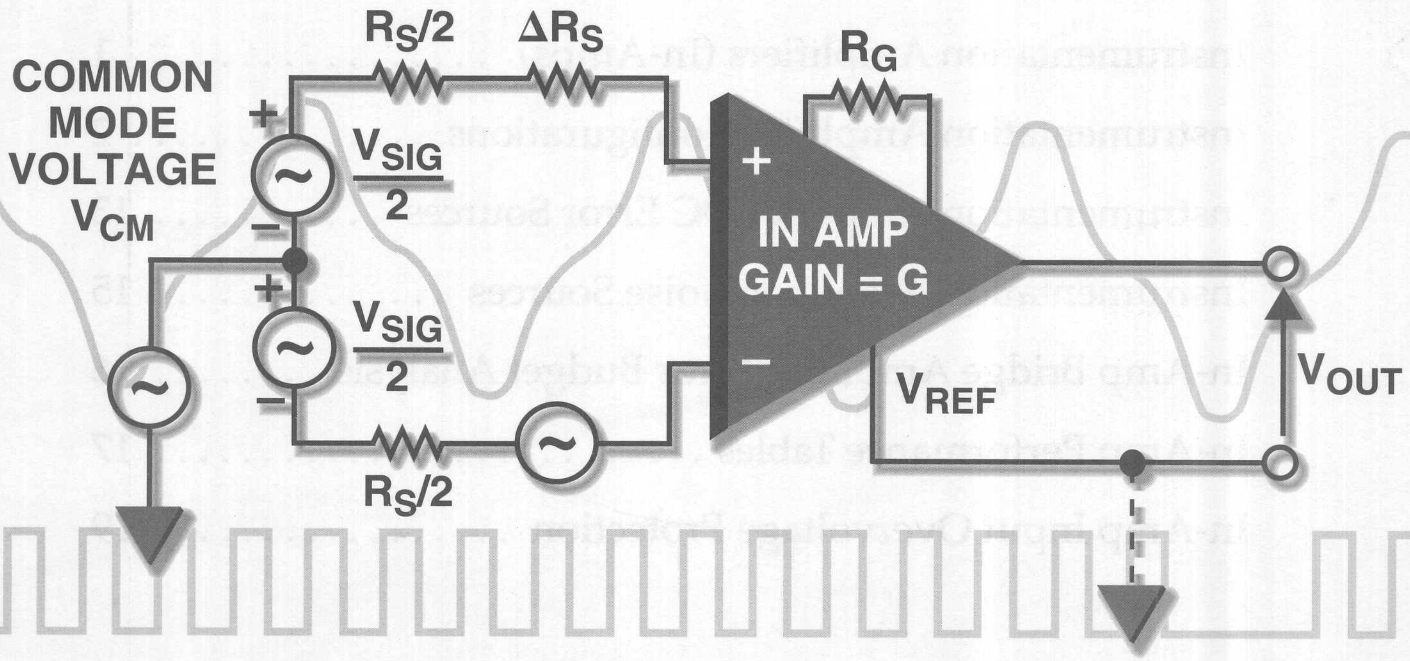
SIGNAL CONDITIONING WITH INSTRUMENTATION AMPLIFIERS



ANALOG DEVICES

Signal Conditioning with Instrumentation Amplifiers

Table of Contents

ANALOG DEVICES

INSTRUMENTATION AMPLIFIERS (IN-AMPS)

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal (see Figure 3.25). The input impedances are balanced and have high values, typically $10^9\Omega$ or higher. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Typical in-amp gain settings range from 1 to 10,000.

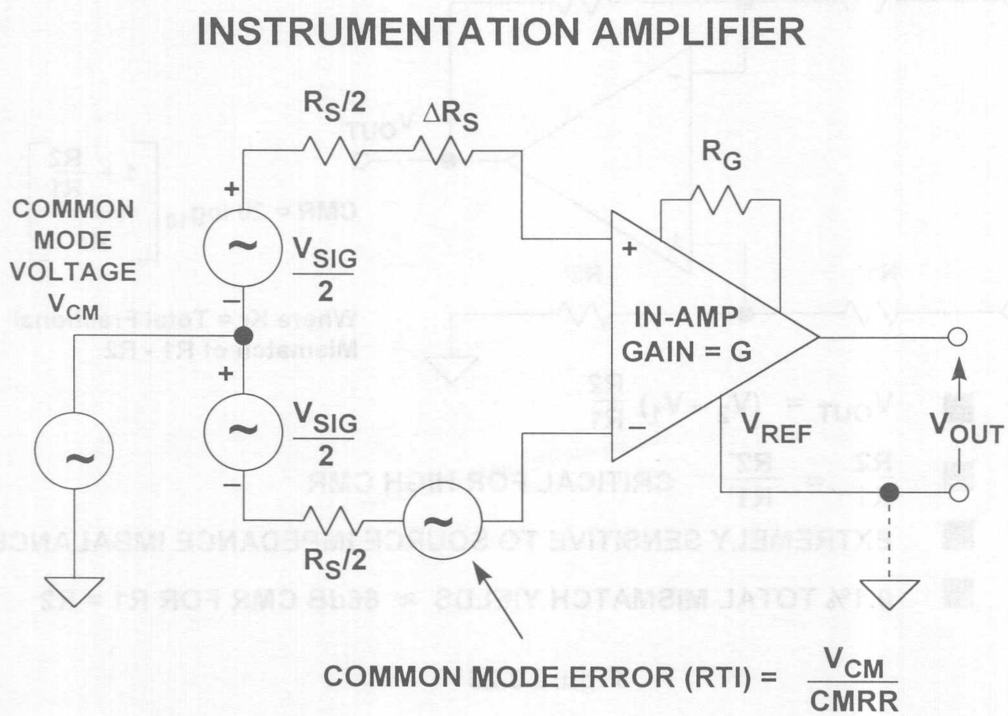


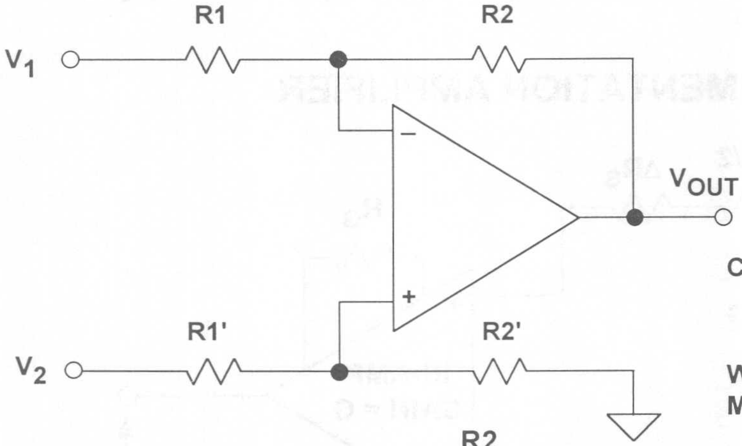
Figure 3.25

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of common mode signal at its inputs. This requires that in-amps have very high common mode rejection (CMR): typical values of CMR are 70dB to over 100dB, with CMR usually improving at higher gains.

It is important to note that a CMR specification for DC inputs alone is not sufficient in most practical applications. In industrial applications, the most common cause of external interference is pickup from the 50/60Hz AC power mains. Harmonics of the power mains frequency can also be troublesome. In differential measurements, this type of interference tends to be induced equally onto both in-amp inputs. The interfering signal therefore appears as a common mode signal to the in-amp. Specifying CMR over frequency is more important than specifying its DC value. Imbalance in the source impedance can degrade the CMR of some in-amps. Analog Devices fully specifies in-amp CMR at 50/60Hz with a source impedance imbalance of 1kΩ.

Low-frequency CMR of op amps, connected as subtractors as shown in Figure 3.26, generally is a function of the resistors around the circuit, not the op amp. A mismatch of only 0.1% in the resistor ratios will reduce the DC CMR to approximately 66dB. Another problem with the simple op amp subtractor is that the input impedances are relatively low and are unbalanced between the two sides. The input impedance seen by V_1 is R_1, but the input impedance seen by V_2 is R1' + R2'. This configuration can be quite problematic in terms of CMR, since even a small source impedance imbalance (~ 10 Ω) will degrade the workable CMR.

OP AMP SUBTRACTOR



$$\text{CMR} = 20\log_{10}\left[\frac{1+\frac{R2}{R1}}{Kr}\right]$$

Where Kr = Total Fractional Mismatch of R1 - R2

- $V_{OUT} = (V_2 - V_1)\,\dfrac{R2}{R1}$
- $\dfrac{R2}{R1} = \dfrac{R2'}{R1'}$ CRITICAL FOR HIGH CMR
- EXTREMELY SENSITIVE TO SOURCE IMPEDANCE IMBALANCE
- 0.1% TOTAL MISMATCH YIELDS ≈ 66dB CMR FOR R1 = R2

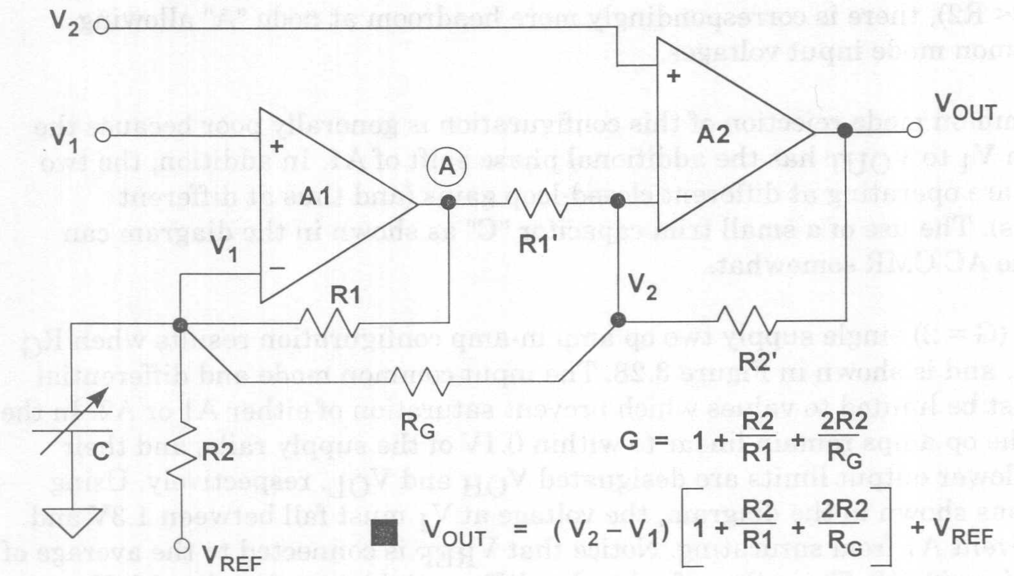
Figure 3.26

Instrumentation Amplifier Configurations

Instrumentation amplifier configurations are based on op amps, but the simple subtractor circuit described above lacks the performance required for precision applications. An in-amp architecture which overcomes some of the weaknesses of the subtractor circuit uses two op amps as shown in Figure 3.27. This circuit is typically referred to as the *two op amp in-amp*. Dual IC op amps are used in most cases for good matching. The circuit gain may be trimmed with an external resistor, R_G. The input impedance is high, permitting the impedance of the signal sources to be high and unbalanced. The DC common mode rejection is limited by the matching of R1/R2 to R1'/R2'. If there is a mismatch in any of the four resistors, the DC common mode rejection is limited to:

$$\text{CMR} \le 20\log\left[\frac{\text{GAIN}\times 100}{\%\text{MISMATCH}}\right].$$

TWO OP AMP INSTRUMENTATION AMPLIFIER



$$G = 1 + \frac{R2}{R1} + \frac{2R2}{R_G}$$

- $V_{OUT} = (V_2 - V_1)\left[1 + \frac{R2}{R1} + \frac{2R2}{R_G}\right] + V_{REF}$
- $\frac{R2}{R1} = \frac{R2'}{R1'}$
- $CMR \leq 20\log\left[\frac{\text{GAIN} \times 100}{\%\ \text{MISMATCH}}\right]$

Figure 3.27

There is an implicit advantage to this configuration due to the gain executed on the signal. This raises the CMR in proportion.

Integrated instrumentation amplifiers are particularly well suited to meeting the combined needs of ratio matching and temperature tracking of the gain-setting resistors. While thin film resistors fabricated on silicon have an initial tolerance of up to ±20%, laser trimming during production allows the ratio error between the resistors to be reduced to 0.01% (100ppm). Furthermore, the tracking between the temperature coefficients of the thin film resistors is inherently low and is typically less than 3ppm/°C (0.0003%/°C).

When dual supplies are used, V_{REF} is normally connected directly to ground. In single supply applications, V_{REF} is usually connected to a low impedance voltage source equal to one-half the supply voltage. The gain from V_{REF} to node "A" is R1/R2, and the gain from node "A" to the output is R2'/R1'. This makes the gain from V_{REF} to the output equal to unity, assuming perfect ratio matching. Note that it is critical that the source impedance seen by V_{REF} be low, otherwise CMR will be degraded.

One major disadvantage of this design is that common mode voltage input range must be traded off against gain. The amplifier A1 must amplify the signal at V_1 by

$$1 + \frac{R1}{R2}.$$

If R1 >> R2 (low gain in Figure 3.27), A1 will saturate if the common mode signal is too high, leaving no headroom to amplify the wanted differential signal. For high gains (R1<< R2), there is correspondingly more headroom at node "A" allowing larger common mode input voltages.

The AC common mode rejection of this configuration is generally poor because the signal from V_1 to V_{OUT} has the additional phase shift of A1. In addition, the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths). The use of a small trim capacitor "C" as shown in the diagram can improve the AC CMR somewhat.

A low gain (G = 2) single supply two op amp in-amp configuration results when R_G is not used, and is shown in Figure 3.28. The input common mode and differential signals must be limited to values which prevent saturation of either A1 or A2. In the example, the op amps remain linear to within 0.1V of the supply rails, and their upper and lower output limits are designated V_{OH} and V_{OL}, respectively. Using the equations shown in the diagram, the voltage at V_1 must fall between 1.3V and 2.4V to prevent A1 from saturating. Notice that V_{REF} is connected to the average of V_{OH} and V_{OL} (2.5V). This allows for bipolar differential input signals with V_{OUT} referenced to +2.5V.

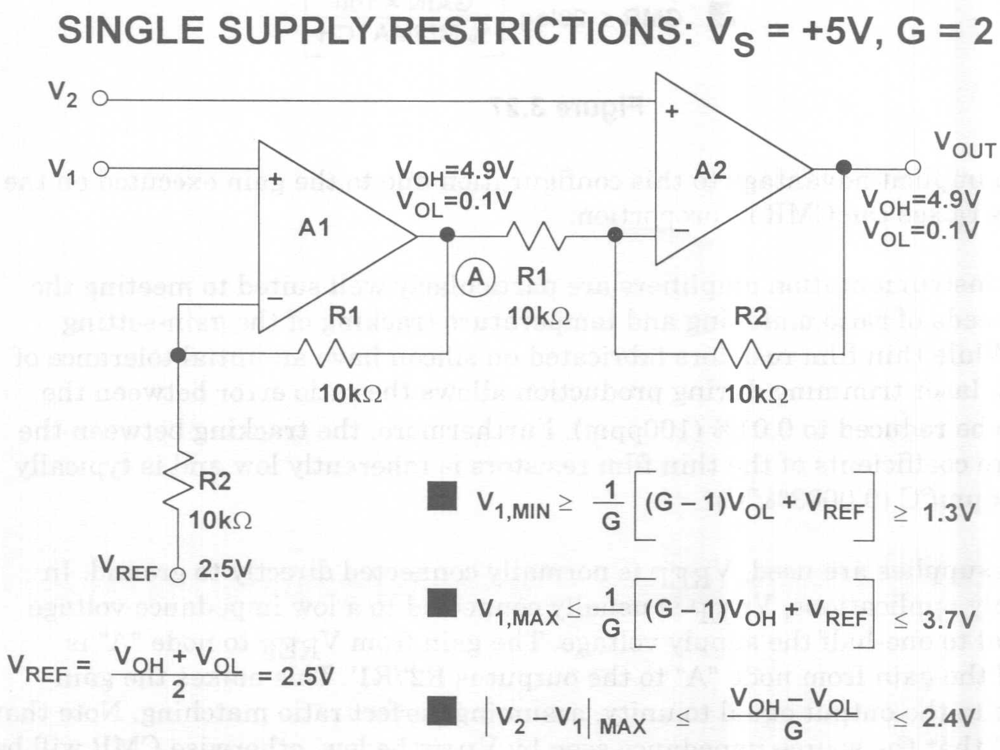
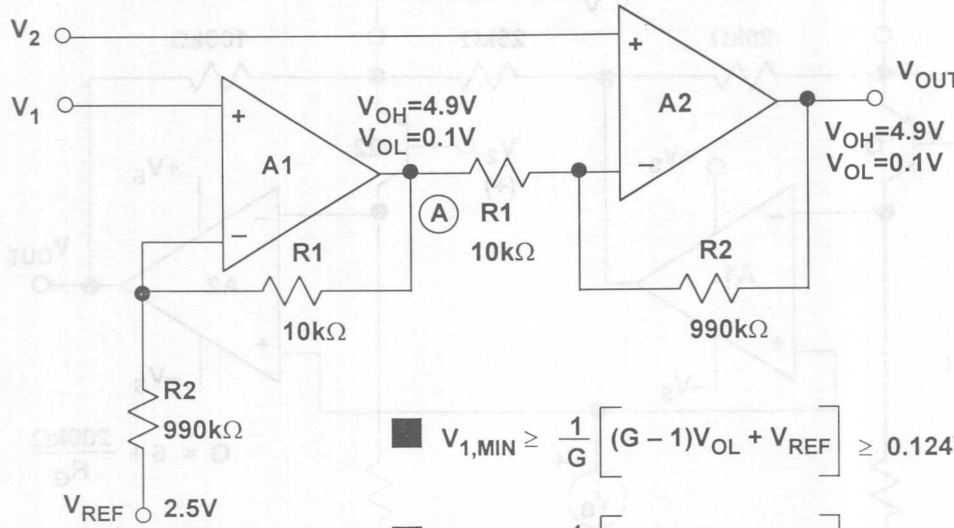


Figure 3.28

A high gain (G = 100) single supply two op amp in-amp configuration is shown in Figure 3.29. Using the same equations, note that the voltage at V_1 can now swing between 0.124V and 4.876V. Again, V_{REF} is connected to 2.5V to allow for bipolar differential input and output signals.

SINGLE SUPPLY RESTRICTIONS: V_S = +5V, G = 100



$$V_{REF} = \frac{V_{OH} + V_{OL}}{2} = 2.5\text{V}$$

- $V_{1,MIN} \geq \frac{1}{G}\left[(G-1)V_{OL} + V_{REF}\right] \geq 0.124\text{V}$
- $V_{1,MAX} \leq \frac{1}{G}\left[(G-1)V_{OH} + V_{REF}\right] \leq 4.876\text{V}$
- $\left|V_2 - V_1\right|_{MAX} \leq \frac{V_{OH} - V_{OL}}{G} \leq 0.048\text{V}$

Figure 3.29

The above discussion shows that regardless of gain, the basic two op amp in-amp does not allow for zero-volt common mode input voltages when operated on a single supply. This limitation can be overcome using the circuit shown in Figure 3.30 which is implemented in the AD627 in-amp. Each op amp is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1 and Q2/A2, respectively. The PNP transistors not only provide gain but also level shift the input signal positive by about 0.5V, thereby allowing the common mode input voltage to go to 0.1V below the negative supply rail. The maximum positive input voltage allowed is 1V less than the positive supply rail.

The AD627 in-amp delivers rail-to-rail output swing and operates over a wide supply voltage range (+2.7V to ±18V). Without R_G, the external gain setting resistor, the in-amp gain is 5. Gains up to 1000 can be set with a single external resistor. Common mode rejection of the AD627B at 60Hz with a 1kΩ source imbalance is 85dB when operating on a single +3V supply and G = 5. Even though the AD627 is a two op amp in-amp, a patented circuit keeps the CMR flat out to a much higher frequency than would be achievable with a conventional discrete two op amp in-amp. The AD627 data sheet (available at http://www.analog.com) has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages. Key specifications for the AD627 are summarized in Figure 3.31.

AD627 IN-AMP ARCHITECTURE

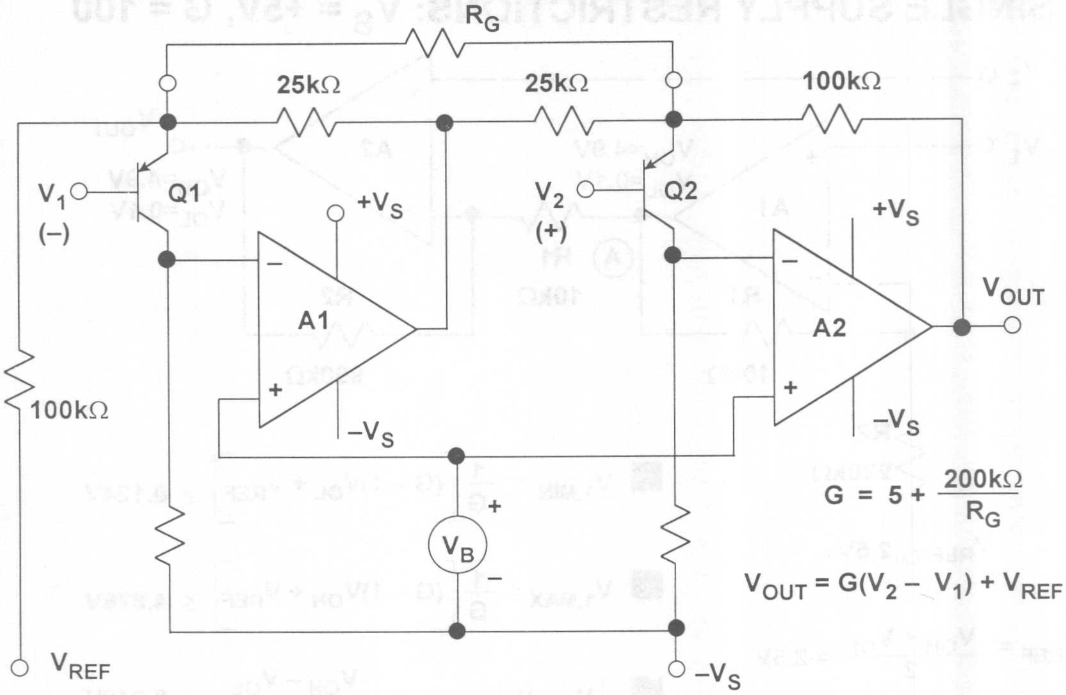


Figure 3.30

AD627 IN-AMP KEY SPECIFICATIONS

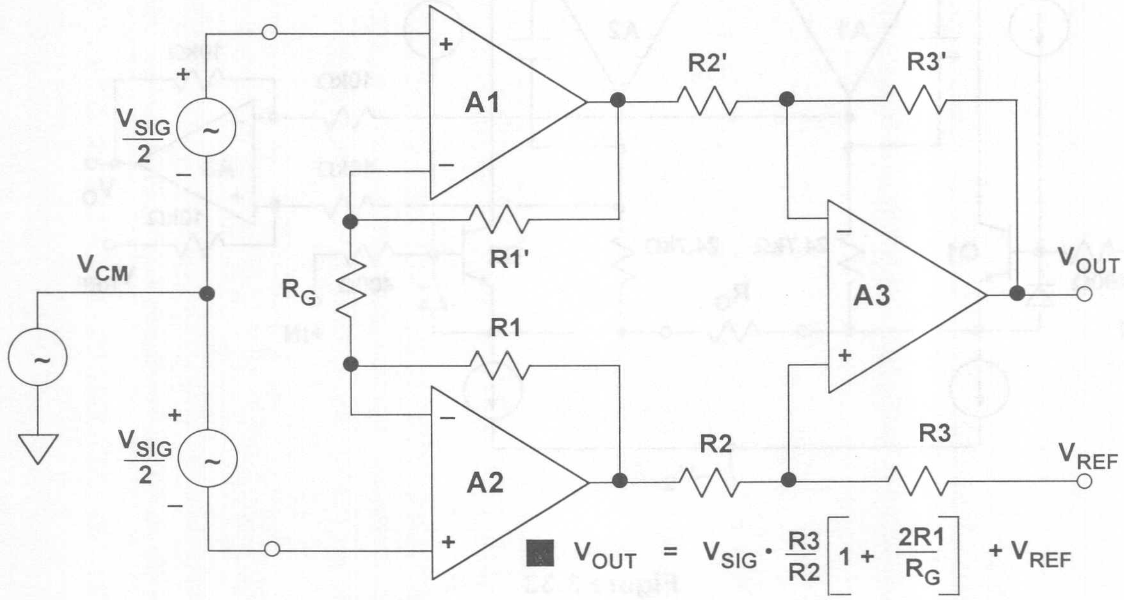
- Wide Supply Range : +2.7V to ±18V
- Input Voltage Range: $-V_S - 0.1V$ to $+V_S - 1V$
- 85µA Supply Current
- Gain Range: 5 to 1000
- 75µV Maximum Input Offset Volage (AD627B)
- 10ppm/°C Maximum Offset Voltage TC (AD627B)
- 10ppm Gain Nonlinearity
- 85dB CMR @ 60Hz, 1kΩ Source Imbalance (G = 5)
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 5)

Figure 3.31

For true balanced high impedance inputs, three op amps may be connected to form the in-amp shown in Figure 3.32. This circuit is typically referred to as the *three op amp in-amp*. The gain of the amplifier is set by the resistor, R_G, which may be internal, external, or (software or pin-strap) programmable. In this configuration, CMR depends upon the ratio matching of R3/R2 to R3'/R2'. Furthermore, common mode signals are only amplified by a factor of 1 regardless of gain (no common mode voltage will appear across R_G, hence, no common mode current will flow in it

because the input terminals of an op amp will have no significant potential difference between them). Thus, CMR will theoretically increase in direct proportion to gain. Large common mode signals (within the A1-A2 op amp headroom limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the popularity of the three op amp in-amp configuration.

THREE OP AMP INSTRUMENTATION AMPLIFIER



- $V_{OUT} = V_{SIG} \cdot \frac{R3}{R2}\left[1 + \frac{2R1}{R_G}\right] + V_{REF}$
- $CMR \leq 20\log\left[\frac{GAIN \times 100}{\%\ MISMATCH}\right]$
- IF R2 = R3, $G = 1 + \frac{2R1}{R_G}$

Figure 3.32

The classic three op amp configuration has been used in a number of monolithic IC instrumentation amplifiers. Besides offering excellent matching between the three internal op amps, thin film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete op amps and resistor networks. The AD620 is an excellent example of monolithic in-amp technology, and a simplified schematic is shown in Figure 3.33.

The AD620 is a highly popular in-amp and is specified for power supply voltages from ±2.3V to ±18V. Input voltage noise is only 9nV/√Hz @ 1kHz. Maximum input bias current is only 1nA maximum because of the Superbeta input stage.

Overvoltage protection is provided by the internal 400Ω thin-film current-limit resistors in conjunction with the diodes which are connected from the emitter-to-base of Q1 and Q2. The gain is set with a single external R_G resistor. The appropriate internal resistors are trimmed so that standard 1% or 0.1% resistors can be used to set the AD620 gain to popular gain values.

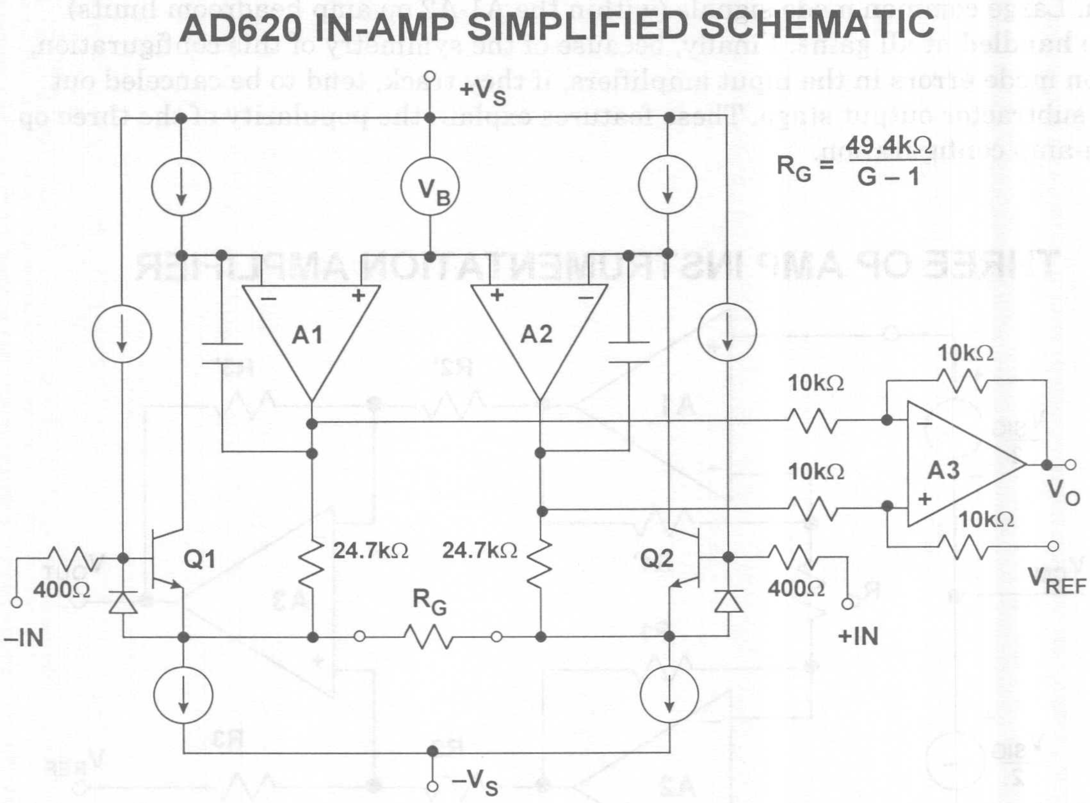


Figure 3.33

As in the case of the two op amp in-amp configuration, single supply operation of the three op amp in-amp requires an understanding of the internal node voltages. Figure 3.34 shows a generalized diagram of the in-amp operating on a single +5V supply. The maximum and minimum allowable output voltages of the individual op amps are designated V_{OH} (maximum high output) and V_{OL} (minimum low output) respectively. Note that the gain from the common mode voltage to the outputs of A1 and A2 is unity, and that *the sum of the common mode voltage and the signal voltage at these outputs must fall within the amplifier output voltage range.* It is obvious that this configuration cannot handle input common mode voltages of either zero volts or +5V because of saturation of A1 and A2. As in the case of the two op amp in-amp, the output reference is positioned halfway between V_{OH} and V_{OL} in order to allow for bipolar differential input signals.

This chapter has emphasized the operation of high performance linear circuits from a single, low-voltage supply (5V or less) is a common requirement. While there are many precision single supply operational amplifiers, such as the OP213, the OP291, and the OP284, and some good single-supply instrumentation amplifiers, the highest performance instrumentation amplifiers are still specified for dual-supply operation.

THREE OP AMP IN-AMP SINGLE +5V SUPPLY RESTRICTIONS

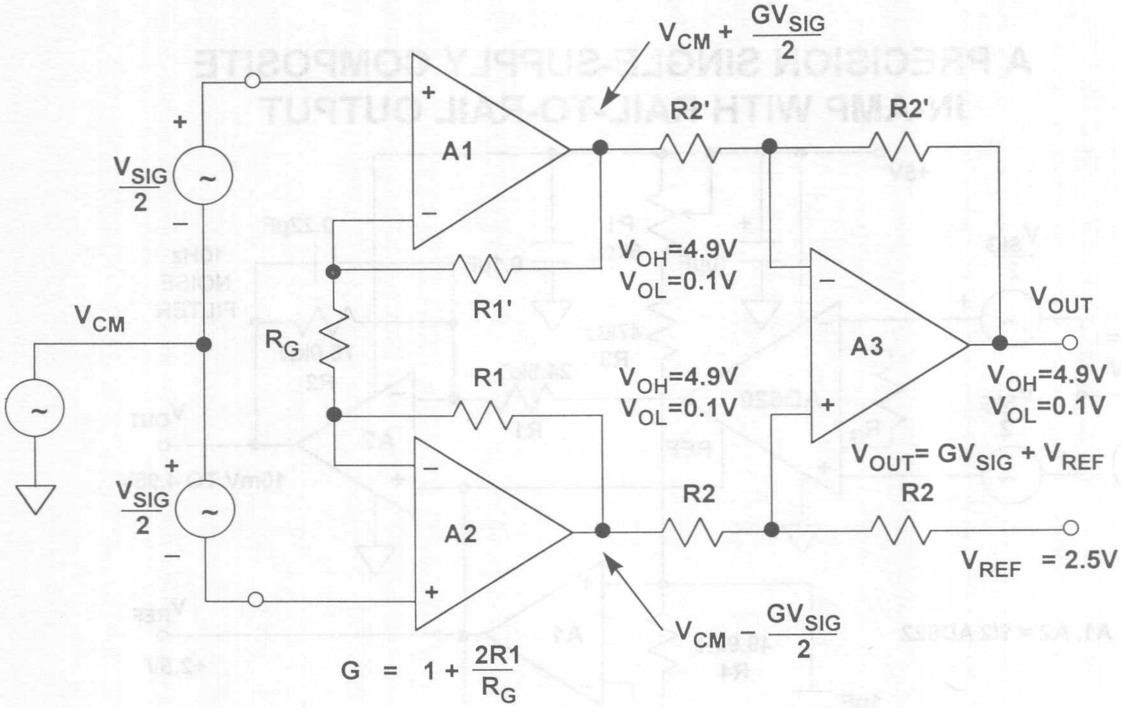


Figure 3.34

One way to achieve both high precision and single-supply operation takes advantage of the fact that several popular sensors (e.g. strain gauges) provide an output signal centered around the (approximate) mid-point of the supply voltage (or the reference voltage), where the inputs of the signal conditioning amplifier need not operate near "ground" or the positive supply voltage.

Under these conditions, a dual-supply instrumentation amplifier referenced to the supply mid-point followed by a "rail-to-rail" operational amplifier gain stage provides very high DC precision. Figure 3.35 illustrates one such high-performance instrumentation amplifier operating on a single, +5V supply. This circuit uses an AD620 low-cost precision instrumentation amplifier for the input stage, and an AD822 JFET-input dual rail-to-rail output operational amplifier for the output stage.

In this circuit, R3 and R4 form a voltage divider which splits the supply voltage in half to +2.5V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of A1, an AD822 which buffers it and provides a low-impedance source needed to drive the AD620's reference pin. The AD620's Reference pin has a 10kΩ input resistance and an input signal current of up to 200μA. The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output

±2.5V, "rail-to-rail," with only ±0.83V required of the AD620. This output voltage level of the AD620 is well within the AD620's capability, thus ensuring high linearity for the "dual-supply" front end. *Note that the final output voltage must be measured with respect to the +2.5V reference, and not to GND.*

A PRECISION SINGLE-SUPPLY COMPOSITE IN-AMP WITH RAIL-TO-RAIL OUTPUT

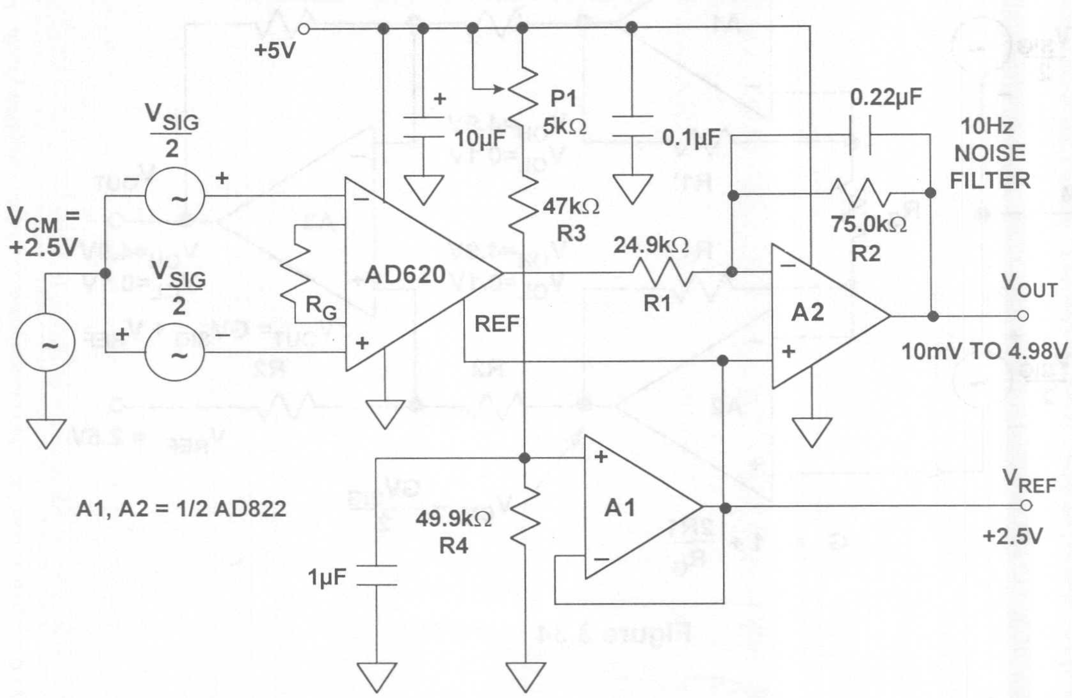


Figure 3.35

The general gain expression for this composite instrumentation amplifier is the product of the AD620 and the inverting amplifier gains:

$$\text{GAIN} = \left(\frac{49.4\text{k}\Omega}{R_G} + 1\right)\left(\frac{R2}{R1}\right)$$

For this example, an overall gain of 10 is realized with $R_G = 21.5\text{k}\Omega$ (closest standard value). The table (Figure 3.36) summarizes various R_G/gain values and performance.

In this application, the allowable input voltage on either input to the AD620 must lie between +2V and +3.5V in order to maintain linearity. For example, at an overall circuit gain of 10, the common mode input voltage range spans 2.25V to 3.25V, allowing room for the ±0.25V full-scale differential input voltage required to drive the output ±2.5V about V_{REF}.

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the A2 stage buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100kHz for gain configurations up to 300. Note that excellent linearity is maintained over 0.1V to 4.9V V_{OUT}. To reduce the effects of unwanted noise pickup, a capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest.

PERFORMANCE SUMMARY OF THE +5V SINGLE-SUPPLY AD620/AD822 COMPOSITE IN-AMP

CIRCUIT GAIN	R_G (Ω)	V_{OS}, RTI (µV)	TC V_{OS}, RTI (µV/°C)	NONLINEARITY (ppm) *	BANDWIDTH (kHz)**
10	21.5k	1000	1000	< 50	600
30	5.49k	430	430	< 50	600
100	1.53k	215	215	< 50	300
300	499	150	150	< 50	120
1000	149	150	150	< 50	30

* Nonlinearity Measured Over Output Range: $0.1V < V_{OUT} < 4.90V$
** Without 10Hz Noise Filter

Figure 3.36

In cases where zero-volt inputs are required, the AD623 single supply in-amp configuration shown in Figure 3.37 offers an attractive solution. The PNP emitter follower level shifters, Q1/Q2, allow the input signal to go 150mV below the negative supply and to within 1.5V of the positive supply. The AD623 is fully specified for single power supplies between +3V and +12V and dual supplies between ±2.5V and ±6V (see Figure 3.38). The AD623 data sheet (available at http://www.analog.com) contains an excellent discussion of allowable input/output voltage ranges as a function of gain and power supply voltages.

AD623 SINGLE-SUPPLY IN-AMP ARCHITECTURE

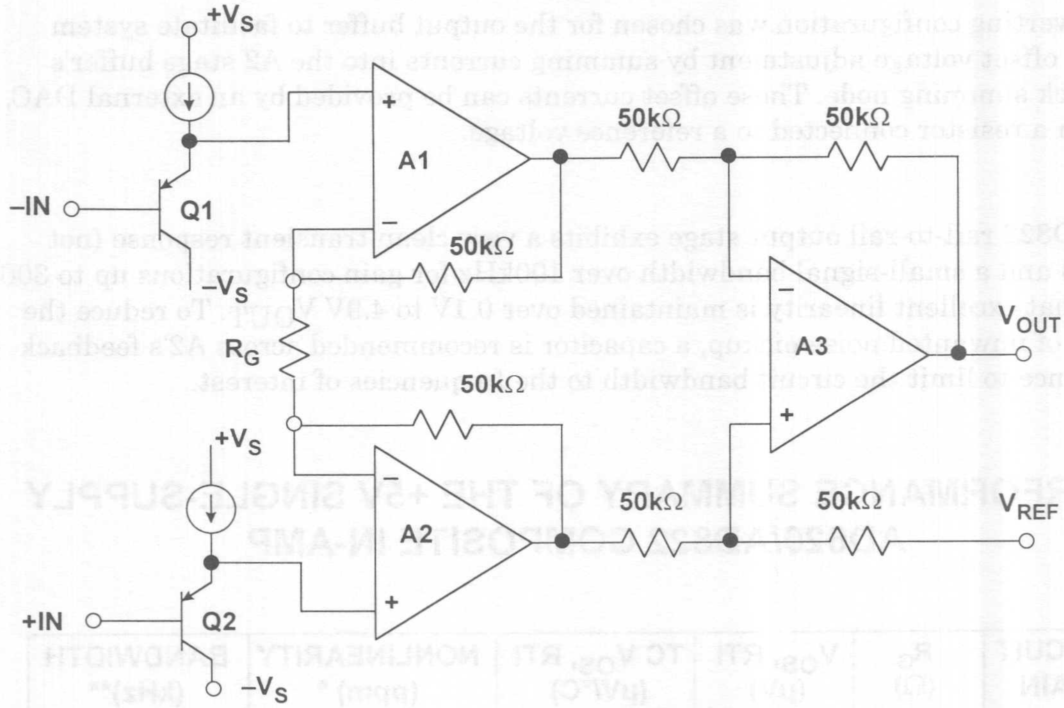


Figure 3.37

AD623 IN-AMP KEY SPECIFICATIONS

- Wide Supply Range: +3V to ±6V
- Input Voltage Range: $-V_S - 0.15V$ to $+V_S - 1.5V$
- 575µA Maximum Supply Current
- Gain Range: 1 to 1000
- 100µV Maximum Input Offset Voltage (AD623B)
- 1µV/°C Maximum Offset Voltage TC (AD623B)
- 50ppm Gain Nonlinearity
- 105dB CMR @ 60Hz, 1kΩ Source Imbalance, G ≥ 100
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 1)

Figure 3.38

Instrumentation Amplifier DC Error Sources

The DC and noise specifications for instrumentation amplifiers differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in-amp is usually set by a single resistor. If the resistor is external to the in-amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC (<25ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5mV input offset voltage becomes 5V at the output for a gain of 10,000. For high gains, the best practice is to use an instrumentation amplifier as a preamplifier then use a post amplifier for further amplification.

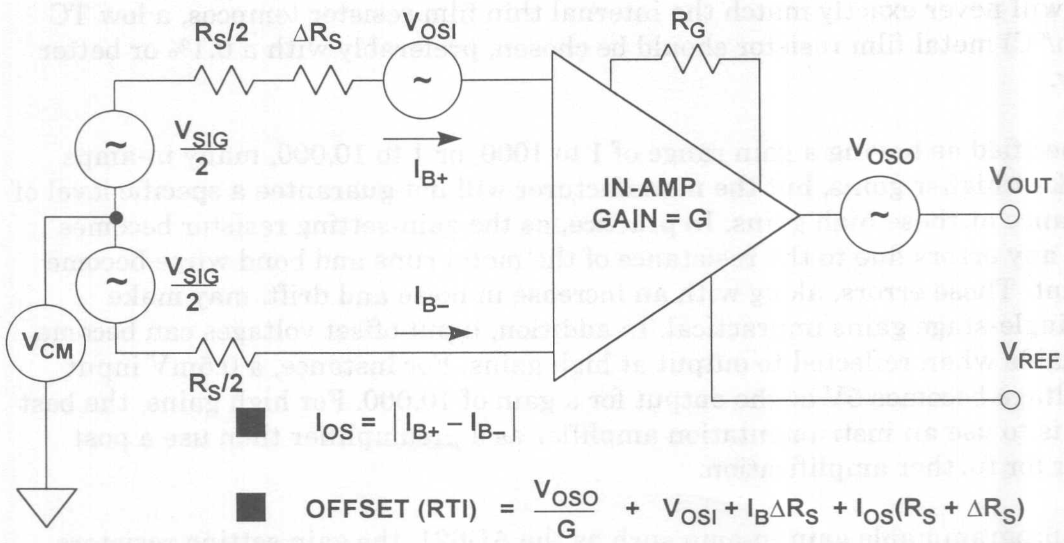
In a pin-programmable gain in-amp such as the AD621, the gain setting resistors are internal, well matched, and the gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD624C have very low factory trimmed gain errors, with its maximum error of 0.02% at G = 1 and 0.25% at G = 500 being typical for this high quality in-amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% (100ppm) or less, and is relatively insensitive to gain over the recommended gain range.

The total input offset voltage of an in-amp consists of two components (see Figure 3.39). Input offset voltage, V_{OSI}, is that component of input offset which is reflected to the output of the in-amp by the gain G. Output offset voltage, V_{OSO}, is independent of gain. At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G=1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In-amp data sheets may specify V_{OSI} and V_{OSO} separately or give the total RTI input offset voltage for different values of gain.

IN-AMP OFFSET VOLTAGE MODEL



- $I_{OS} = |I_{B+} - I_{B-}|$
- $\text{OFFSET (RTI)} = \dfrac{V_{OSO}}{G} + V_{OSI} + I_B \Delta R_S + I_{OS}(R_S + \Delta R_S)$
- $\text{OFFSET (RTO)} = V_{OSO} + G\left[V_{OSI} + I_B \Delta R_S + I_{OS}(R_S + \Delta R_S)\right]$

Figure 3.39

Input bias currents may also produce offset errors in in-amp circuits (see Figure 3.39). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), then there is an additional input offset voltage error due to the bias current, equal to $I_B \Delta R_S$ (assuming that $I_{B+} \approx I_{B-} = I_B$). This error is reflected to the output, scaled by the gain G. The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S + \Delta R_S$, equal to $I_{OS}(R_S + \Delta R_S)$, which is also reflected to the output by the gain, G.

In-amp common mode error is a function of both gain and frequency. Analog Devices specifies in-amp CMR for a 1kΩ source impedance unbalance at a frequency of 60Hz. The RTI common mode error is obtained by dividing the common mode voltage, V_{CM}, by the common mode rejection ratio, CMRR.

Power supply rejection (PSR) is also a function of gain and frequency. For in-amps, it is customary to specify the sensitivity to each power supply separately. Now that all DC error sources have been accounted for, a worst case DC error budget can be calculated by reflecting all the sources to the in-amp input (Figure 3.40).

INSTRUMENTATION AMPLIFIER AMPLIFIER DC ERRORS REFERRED TO THE INPUT (RTI)

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy × FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{OSI}	V_{OSI}
Output Offset Voltage, V_{OSO}	$V_{OSO} \div G$
Input Bias Current, I_B, Flowing in ΔR_S	$I_B \Delta R_S$
Input Offset Current, I_{OS}, Flowing in R_S	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, V_{CM}	$V_{CM} \div CMRR$
Power Supply Variation, ΔV_S	$\Delta V_S \div PSRR$

Figure 3.40

Instrumentation Amplifier Noise Sources

Since in-amps are primarily used to amplify small precision signals, it is important to understand the effects of all the associated noise sources. The in-amp noise model is shown in Figure 3.41. There are two sources of input voltage noise. The first is represented as a noise source, V_{NI}, in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in-amp gain, G. The second noise source is the output noise, V_{NO}, represented as a noise voltage in series with the in-amp output. The output noise, shown here referred to V_{OUT}, can be referred to the input by dividing by the gain, G.

There are two noise sources associated with the input noise currents I_{N+} and I_{N-}. Even though I_{N+} and I_{N-} are usually equal ($I_{N+} \approx I_{N-} = I_N$), they are uncorrelated, and therefore, the noise they each create must be summed in a root-sum-squares (RSS) fashion. I_{N+} flows through one half of R_S, and I_{N-} the other half. This generates two noise voltages, each having an amplitude, $I_N R_S/2$. Each of these two noise sources is reflected to the output by the in-amp gain, G.

The total output noise is calculated by combining all four noise sources in an RSS manner:

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{V_{NO}^2 + G^2\left(V_{NI}^2 + \frac{I_{N+}^2 R_S^2}{4} + \frac{I_{N-}^2 R_S^2}{4}\right)}.$$

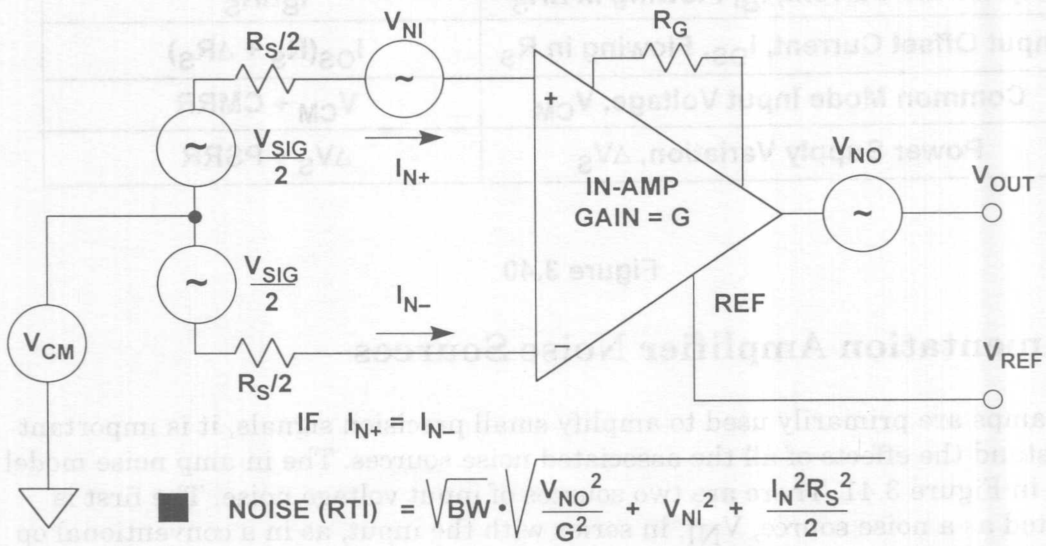
If $I_{N+} = I_{N-} = I_N$,

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{V_{NO}{}^2 + G^2\left(V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}\right)}$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in-amp gain, G:

$$\text{NOISE (RTI)} = \sqrt{BW}\sqrt{\frac{V_{NO}{}^2}{G^2} + \left(V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}\right)}.$$

IN-AMP NOISE MODEL



- $\text{NOISE (RTI)} = \sqrt{BW \cdot}\sqrt{\frac{V_{NO}{}^2}{G^2} + V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}}$
- $\text{NOISE (RTO)} = \sqrt{BW \cdot}\sqrt{V_{NO}{}^2 + G^2\left[V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}\right]}$
- BW = 1.57 × IN-AMP Bandwidth @ Gain = G

Figure 3.41

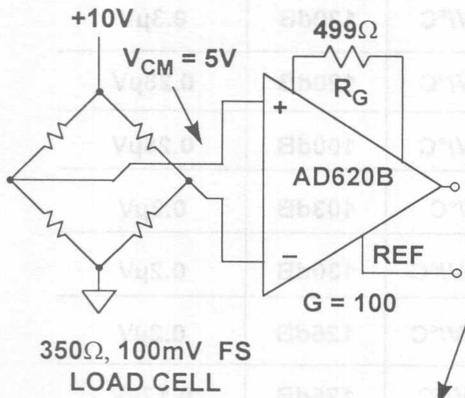
In-amp data sheets often present the total voltage noise RTI as a function of gain. This noise spectral density includes both the input (V_{NI}) and output (V_{NO}) noise contributions. The input current noise spectral density is specified separately. As in the case of op amps, the total noise RTI must be integrated over the in-amp closed-loop bandwidth to compute the RMS value. The bandwidth may be determined from data sheet curves which show frequency response as a function of gain.

In-Amp Bridge Amplifier Error Budget Analysis

It is important to understand in-amp error sources in a typical application. Figure 3.42 shows a 350Ω load cell which has a fullscale output of 100mV when excited with a 10V source. The AD620 is configured for a gain of 100 using the external

499Ω gain-setting resistor. The table shows how each error source contributes to the total unadjusted error of 2145ppm. The gain, offset, and CMR errors can be removed with a system calibration. The remaining errors - gain nonlinearity and 0.1Hz to 10Hz noise - cannot be removed with calibration and limit the system resolution to 42.8ppm (approximately 14-bit accuracy).

AD620B BRIDGE AMPLIFIER DC ERROR BUDGET



MAXIMUM ERROR CONTRIBUTION, +25°C
FULLSCALE: V_{IN} = 100mV, V_{OUT} = 10V

V_{OS}	55µV ÷ 100mV	550ppm
I_{OS}	350Ω × 0.5nA ÷ 100mV	1.8ppm
Gain Error	0.15%	1500ppm
Gain Nonlinearity	40ppm	40ppm
CMR Error	120dB 1ppm × 5V ÷ 100mV	50ppm
0.1Hz to 10Hz 1/f Noise	280nV ÷ 100mV	2.8ppm
Total Unadjusted Error	≈ 9 Bits Accurate	2145ppm
Resolution Error	≈ 14 Bits Accurate	42.8ppm

AD620B SPECS @ +25°C, ±15V
$V_{OSI} + V_{OSO}/G$ = 55µV max
I_{OS} = 0.5nA max
Gain Error = 0.15%
Gain Nonlinearity = 40ppm
0.1Hz to 10Hz Noise = 280nVp-p
CMR = 120dB @ 60Hz

Figure 3.42

In-Amp Performance Tables

Figure 3.43 shows a selection of precision in-amps designed primarily for operation on dual supplies. It should be noted that the AD620 is capable of single +5V supply operation (see Figure 3.35), but neither its input nor its output are capable of rail-to-rail swings.

Instrumentation amplifiers specifically designed for single supply operation are shown in Figure 3.44. It should be noted that although the specifications in the figure are given for a single +5V supply, all of the amplifiers are also capable of dual supply operation and are specified for both dual and single supply operation on their data sheets. In addition, the AD623 and AD627 will operate on a single +3V supply.

The AD626 is not a true in-amp but is a differential amplifier with a thin-film input attenuator which allows the common mode voltage to exceed the supply voltages. This device is designed primarily for high and low-side current-sensing applications. It will also operate on a single +3V supply.

PRECISION IN-AMPS: DATA FOR V_S = ±15V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise
AD524C	0.5% / P	100ppm	50µV	0.5µV/°C	120dB	0.3µV
AD620B	0.5% / R	40ppm	50µV	0.6µV/°C	120dB	0.28µV
AD621B[1]	0.05% / P	10ppm	50µV	1.6µV/°C	100dB	0.28µV
AD622	0.5% / R	40ppm	125µV	1µV/°C	103dB	0.3µV
AD624C[2]	0.25% / R	50ppm	25µV	0.25µV/°C	130dB	0.2µV
AD625C	0.02% / R	50ppm	25µV	0.25µV/°C	125dB	0.2µV
AMP01A	0.6% / R	50ppm	50µV	0.3µV/°C	125dB	0.12µV
AMP02E	0.5% / R	60ppm	100µV	2µV/°C	115dB	0.4µV

* / P = Pin Programmable
* / R = Resistor Programmable

1 G = 100
2 G = 500

Figure 3.43

SINGLE SUPPLY IN-AMPS: DATA FOR V_S = +5V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise	Supply Current
AD623B	0.5% / R	50ppm	100µV	1µV/°C	105dB	1.5µV	575µA
AD627B	0.35% / R	10ppm	75µV	1µV/°C	85dB	1.5µV	85µA
AMP04E	0.4% / R	250ppm	150µV	3µV/°C	90dB	0.7µV	290µA
AD626B[1]	0.6% / P	200ppm	2.5mV	6µV/°C	80dB	2µV	700µA

* / P = Pin Programmable
* / R = Resistor Programmable

1 Differential Amplifier, G = 100

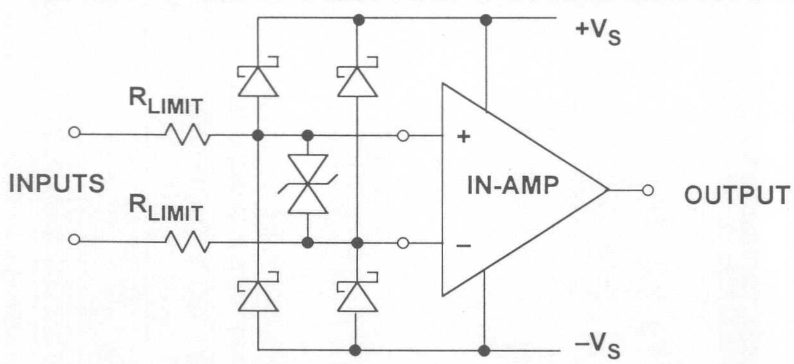
Figure 3.44

In-Amp Input Overvoltage Protection

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in-amps have absolute maximum input voltage specifications equal to $\pm V_S$. External series resistors (for current limiting) and Schottky diode clamps may be used to prevent overload, if necessary. Some instrumentation amplifiers have built-in overload protection circuits in the form of series resistors (thin film) or series-protection FETs. In-amps such as the AMP-02 and the AD524 utilize series-protection FETs, because they act as a low impedance during normal operation, and a high impedance during fault conditions.

An additional Transient Voltage Suppresser (TVS) may be required across the input pins to limit the maximum differential input voltage. This is especially applicable to three op amp in-amps operating at high gain with low values of R_G. A more detailed discussion of input voltage and EMI/RFI protection can be found in Section 10 of this book.

INSTRUMENTATION AMPLIFIER
INPUT OVERVOLTAGE CONSIDERATIONS



- **Always Observe Absolute Maximum Data Sheet Specs!**
- **Schottky Diode Clamps to the Supply Rails Will Limit Input to Approximately $\pm V_S$ ±0.3V, TVSs Limit Differential Voltage**
- **External Resistors (or Internal Thin-Film Resistors) Can Limit Input Current, but will Increase Noise**
- **Some In-Amps Have Series-Protection Input FETs for Lower Noise and Higher Input Over-Voltages (up to ±60V, Depending on Device)**

Figure 3.45

Notes